What is claimed is:

1. A method of reading data in a ferroelectric memory device, comprising:

applying a read voltage to a ferroelectric capacitor; and

detecting a voltage that reflects an amount of a dynamic change in capacitance of the ferroelectric capacitor to which the read voltage is applied.

2. The method of reading data in a ferroelectric memory device as defined in claim 1,

wherein the ferroelectric capacitor stores one of first data and second data, the first data being stored based on spontaneous polarization of a first polarity when a voltage applied to the ferroelectric capacitor is returned from a write voltage of the first polarity to 0 V, the second data being stored based on spontaneous polarization of a second polarity when the voltage applied to the ferroelectric capacitor is returned from a write voltage of the second polarity to 0 V, and

wherein polarity of polarization of the ferroelectric capacitor which has stored the first data is not reversed, and polarity of polarization of the ferroelectric capacitor which has stored the second data is reversed, when a voltage of the first polarity is applied to the ferroelectric capacitor as the read voltage.

3. The method of reading data in a ferroelectric memory device as defined in claim 2,

wherein the dynamic change in the capacitance of the ferroelectric capacitor which has stored the second data is greater than the dynamic change in the capacitance of the ferroelectric capacitor which has stored the first data, when a voltage of the first polarity is applied to the ferroelectric capacitor as the read voltage.

4. The method of reading data in a ferroelectric memory device as defined in claim 1,

wherein a voltage-rise curve includes a portion in which a voltage-rise gradient differs depending on whether a polarization value of the ferroelectric capacitor is a first value or a second value, the voltage-rise curve indicating a voltage rise of a sense line connected with the ferroelectric capacitor when the read voltage is applied to the ferroelectric capacitor, and a timing of detecting the voltage that reflects the amount of the dynamic change is set in a period specified by the portion in which the voltage-rise gradient differs.

5. The method of reading data in a ferroelectric memory device as defined in claim 2,

wherein the voltage that reflects the amount of the dynamic change is detected when the read voltage is applied to the ferroelectric capacitor which has stored the second data, around a time at which the polarization of the ferroelectric capacitor becomes zero in a hysteresis characteristic between polarization and an applied voltage of the ferroelectric capacitor.

6. A ferroelectric memory device comprising:

voltage applying section which applies a read voltage to a ferroelectric capacitor; and

voltage detection section which detects a voltage that reflects an amount of a dynamic change in capacitance of the ferroelectric capacitor to which the read voltage is applied.

7. The ferroelectric memory device as defined in claim 6,

wherein a voltage-rise curve includes a portion in which a voltage-rise gradient

differs depending on whether a polarization value of the ferroelectric capacitor is a first value or a second value, the voltage-rise curve indicating a voltage rise of a sense line connected with the ferroelectric capacitor when the read voltage is applied to the ferroelectric capacitor, and a timing of detecting the voltage that reflects the amount of the dynamic change by the voltage detection section is set in a period specified by the portion in which the voltage-rise gradient differs.

8. A ferroelectric memory device comprising:

a plurality of memory cells, each of the memory cells including a ferroelectric capacitor and a switching element;

a plurality of wordlines, each of the wordlines extending in a first direction and being connected in common with a control terminal of the switching element in each of the memory cells arranged along the first direction;

a plurality of bitlines, each of the bitlines extending in a second direction and being connected in common with one end of the switching element in each of the memory cells arranged along the second direction, the second direction intersecting the first direction;

a plurality of sense lines, each of the sense lines extending in the second direction and being connected in common with one end of the ferroelectric capacitor and the other end of the switching element in each of the memory cells arranged in the second direction;

a plurality of plate lines, each of the plate lines extending in the first direction and being connected in common with the other end of the ferroelectric capacitor in each of the memory cells arranged in the first direction; and

a voltage detection section which detects a voltage of the sense lines in a specified period, when a read voltage is applied to the ferroelectric capacitor of at least one selected memory cell selected from among the plurality of memory cells, the specified period

being specified by a portion of a voltage-rise curve in which a voltage-rise gradient differs depending on whether a polarization value of the ferroelectric capacitor is a first value or a second value, and the voltage-rise curve indicating a voltage rise of one of the sense lines connected with the ferroelectric capacitor of the selected memory cell.

9. The ferroelectric memory device as defined in claim 8, further comprising:

a read timing generation device which generates a timing signal for setting a period for detecting the voltage of the sense lines,

wherein the voltage detection section includes a plurality of sense amplifiers connected with the sense lines, and

wherein the read timing generation device activates the sense amplifiers by outputting the timing signal to the sense amplifiers.

10. The ferroelectric memory device as defined in claim 8,

wherein, when reading or writing data, the switching element in the selected memory cell is turned on by applying a selected-wordline voltage to a selected wordline which is a wordline among the plurality of the wordlines and to be used for selecting the selected memory cell, and the switching element in an unselected memory cell among the plurality of the memory cells is turned off by applying an unselected-wordline voltage to an unselected wordline which is a wordline other than the selected wordline among the plurality of the wordlines, and

wherein a read plate-line voltage or a write plate-line voltage is applied to a selected plate line which is a plate line among the plurality of the plate lines and connected with the selected memory cell, and an unselected plate line, which is a plate line other than the selected plate line among the plurality of the plate lines, is set in a floating state.

11. The ferroelectric memory device as defined in claim 8,

wherein, when reading data, a read bitline voltage is applied to a selected bitline which is a bitline among the plurality of bitlines and connected with the selected memory cell, and an unselected-bitline voltage is applied to an unselected bitline which is a bitline other than the selected bitline among the plurality of the bitlines.

12. The ferroelectric memory device as defined in claim 10,

wherein, when writing data "1", a data "1" write bitline voltage is applied to a selected bitline which is a bitline among the plurality of bitlines and connected with the selected memory cell, an unselected-bitline voltage is applied to an unselected bitline which is a bitline other than the selected bitline among the plurality of the bitlines, and a data "1" write plate-line voltage is applied to the selected plate line.

13. The ferroelectric memory device as defined in claim 10,

wherein, when writing data "0", a data "0" write bitline voltage is applied to a selected bitline which is a bitline among the plurality of bitlines and connected with the selected memory cell, an unselected-bitline voltage is applied to an unselected bitline which is a bitline other than the selected bitline among the plurality of the bitlines, and a data "0" write plate-line voltage is applied to the selected plate line.

14. The ferroelectric memory device as defined in claim 9,

wherein each of the sense amplifiers activated for a predetermined period of time by the timing signal compares a cell voltage from one of the sense lines with a reference voltage.